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APPLICATION FOR LETTERS PATENT

FOR

DEVICE ISOLATION FOR SEMICONDUCTOR DEVICES

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DEVICE ISOLATION FOR SEMICONDUCTOR DEVICES

Field of the Invention

This invention relates to semiconductor fabrication processing and more particularly to a method for forming isolation for Complimentary Metal Oxide Semiconductor (CMOS) devices.

Background of the Invention

The continuing trend of scaling down integrated circuits has forced the semiconductor industry to consider new techniques for fabricating smaller components at sub-micron levels. With the industry moving towards processes for fabrication of smaller device geometries, isolation between devices becomes a very critical issue.

Several isolation methods are currently prevalent in the semiconductor industry. One method, LOCal Oxidation of Silicon (LOCOS) uses patterned silicon nitride as an oxidation inhibitor so that the silicon substrate will oxidize where the nitride is removed and not oxidize where the nitride is present. A main fabrication concern when using LOCOS is the encroachment of oxide under the nitride that causes the well known "bird's-beak" problem.

A second isolation method is deep trench isolation, where a single deep trench is etched into the silicon substrate and then filled with oxide. However, deep trenches have proven difficult to reliably manufacture over an entire wafer and the width of the trench is limited to the critical dimension of a given process.

The present invention develops a method to fabricate device isolation for sub-micron fabrication processes. In particular, the present invention provides a device isolation method for processes using a device geometry of 0.18μm or smaller.

Summary of the Invention

An exemplary implementation of the present invention discloses an isolation structure and processes for fabricating the isolation structure for a semiconductor device.

In a general aspect of the present invention, a semiconductor assembly having at least one isolation structure is formed. The semiconductor assembly may simply comprise a trench in a semiconductive substrate, the trench being filled with an insulation material. In a preferred general embodiment, the semiconductor assembly comprises: a first trench in a semiconductive substrate; a second trench extending the overall trench depth in the semiconductive substrate by being aligned to the first trench; and an insulation material substantially filling the first and second trenches. The isolation structure separates a non-continuous surface of a conductive region.

General process steps to form the isolation structure comprise: forming a mask over a semiconductor substrate assembly; forming a first trench into the semiconductor substrate assembly using the mask as an etching guide; forming an insulation layer on the surface of the first trench; forming a semiconductive spacer on the side wall of the first trench; forming a second trench into the semiconductor substrate assembly at the bottom of the first trench by using the semiconductive spacer as an etching guide; forming an isolation filler in the first and second trenches, the isolation filler substantially consuming the semiconductive spacer and thereby substantially filling the first and second trenches; and planarizing the isolation filler. If sufficient for a given process, the steps to form a second trench could be skipped and the isolation filler would then be formed in a first trench.

Brief Description of the Drawings

Figure 1A is a cross-sectional view depicting a semiconductor substrate covered with a first insulation layer and a patterned masking material.

Figure 1B is a subsequent cross-sectional view taken from Figure 1A depicting an etching step that forms a first trench into the semiconductive substrate.

Figure 1C is a subsequent cross-sectional view taken from Figure 1B depicting the removal of the patterned masking layer, the formation of a second insulation layer and the formation of a semiconductive layer.

Figure 1D is a subsequent cross-sectional view taken from Figure 1C depicting an etching step to form semiconductive spacers on the wall of the first trench.

Figure 1E is a subsequent cross-sectional view taken from Figure 1D depicting a second etching step to form a second trench into the semiconductive substrate.

Figure 1F is a subsequent cross-sectional view taken from Figure 1E depicting the formation of an isolation material that consumes the semiconductive spacers and fills both the first and second substrate trenches.

Figure 1G is a subsequent cross-sectional view taken from Figure 1F showing the isolation material after planarization.

Figure 1H is an expanded cross-sectional view taken from Figure 1F showing the isolation structure in relationship to bordering transistor devices.

Figure 2A is a cross-sectional view depicting a semiconductor substrate covered with a first insulation layer and a patterned masking material.

Figure 2B is a subsequent cross-sectional view taken from Figure 2A depicting an etching step that forms a first trench into the semiconductive substrate.

Figure 2C is a subsequent cross-sectional view taken from Figure 2B depicting the removal of the patterned masking layer, the formation of a second insulation layer and the formation of a semiconductive layer.

Figure 2D is a subsequent cross-sectional view taken from Figure 2C depicting an etching step to form a semiconductive spacer on the wall of the first trench.

Figure 2E is a subsequent cross-sectional view taken from Figure 2D depicting a second etching step to form a second trench into the semiconductive substrate.

Figure 2F is a subsequent cross-sectional view taken from Figure 2E, following the formation of a conformal polysilicon layer into the first and second trenches.

Figure 2G is a subsequent cross-sectional view taken from Figure 2F depicting the formation of an isolation material that consumes the semiconductive spacer, conformal polysilicon (if present) and fills both the first and second substrate trenches.

Figure 2H is a subsequent cross-sectional view taken from Figure 2G showing the isolation material after planarization.

Figure 2I is an expanded cross-sectional view taken from Figure 2H showing the isolation structure in relationship to bordering transistor devices.

Detailed Description of the Invention

Exemplary implementations of the present invention are directed to an isolation structure and a process for forming semiconductor device isolation as depicted in the embodiments of Figures 1A-1H and Figures 2A-2I.

Referring to Figure 1A, a semiconductive substrate 10, such as a silicon wafer, is prepared for the processing steps of the present invention. A first insulation layer 11, such as oxide, covers the surface of semiconductive substrate 10. It is preferred to form the oxide by growing the oxide on the semiconductive substrate. A masking material 12, such as photoresist, is patterned over semiconductive substrate 10 leaving an exposed portion of insulation layer 11.

Referring now to Figure 1B, an anisotropic etch is performed that etches through the exposed portion of insulation layer 11 and continues into the semiconductive substrate 10 to form a first trench 13 therein. The desired depth of first trench 13 is discussed further in the process steps.

Referring now to Figure 1C, the masking material 12 is stripped from the substrate's surface. Next, a second insulation layer 14 is formed over the remaining first insulation layer 11 and next to first trench 13. The second insulation layer 14 may be oxide formed by subjecting the trenched area of the substrate to oxidation. Next, conformal layer of semiconductive material 15, such as polysilicon, is deposited on the second insulation layer 14. The thickness of semiconductive material 15, represented by either forming the

layer to thickness 15A or 15B, will determine the width of a subsequently etched trench. It is preferred that semiconductive material 15 be approximately one fourth (or less) the width of first trench 13. This ratio will enable the formation of a subsequently formed second trench to a desired width. Also, material 15 may be any material that is oxidizable with silicon being the preferred material, as most semiconductor processes and particularly DRAM processes readily use silicon.

Referring now to Figure 1D, semiconductive material 15 is anisotropically etched to remove the material from the bottom of trench 13 and simultaneously from the upper surface of the substrate. This anisotropic etch will leave behind semiconductive material spacer 16A or 16B (again depending on the thickness of semiconductive material 15) on the side wall of first trench 13, expose portions of insulation layer 14 at the bottom of first trench 13 and also expose portions on the upper surface of the substrate. During this anisotropic etch (or spacer etch in this case), as semiconductive material spacer 16A or 16B is formed, the spacer etch will completely clear the semiconductive material from the non-trenched wafer surface as well as clear the material from a portion of wafer surface at the bottom of the trench. The semiconductive material spacer (16A or 16B) is easily formed as an anisotropic etch basically removes material in a generally vertical direction and thereby leaves behind a vertical spacer that lines the wall along the circumference of first trench 13 and removes semiconductive material at the bottom of first trench 13.

Referring now to Figure 1E, an anisotropic etch (either the continuation of the previous anisotropic spacer etch described in Figure 1D or a separate anisotropic etch) is performed that etches into the substrate using the semiconductive material spacer (16 A or 16B) as a self-aligning guide. This etch will also remove more of the spacer material, however a desired trench depth is easily reached while a substantial portion of the spacer material remains intact. Note, as stated previously, the thickness of the spacer can easily be used to define the trench opening and thus the width and depth of the trench (as shown in Figure 1E).

Referring now to Figure 1F, isolation material 18 is formed such that it consumes the semiconductive spacer (16A or 16B), insulation layer 14 and fills both the first and second substrate trenches (13 and 17A or 17B). In order to form isolation material

18, it is preferred to anneal the entire semiconductor assembly in a furnace while providing an oxidizing agent to the semiconductor assembly. In a preferred embodiment, the semiconductive substrate is silicon and the semiconductive spacer is polysilicon. Polysilicon will oxidize at a faster rate than the silicon substrate, so the oxidation of the silicon substrate along the edges of the trench is minimized by the time the polysilicon is substantially (completely) oxidized. Isolation material 18 may also be formed by the deposition of oxide to fill the trenches.

At this point in the process, and referring now to Figure 1G, isolation material 18 may be planarized to substantially reduce or possibly even eliminate any encroachment of isolation material 18 at the upper corners of first trench 13. This planarization step would also prepare the semiconductor assembly for further processing, such as for transistor formation. In this embodiment, chemical mechanical planarization (CMP) is preferred as there are no etch stop layers available to facilitate use of an etch to planarize isolation material 18.

Figure 1G shows a relationship between the formed isolation structure 18 and bordering transistors 19. Transistors 19 comprise of transistor gates 19B bridging across diffusion regions 19A. This view demonstrates the importance of second trench 17 to obtain effective isolation between transistors 19. It is preferred that the overall depth of first trench 13 and second trench 17 be two times the depth of diffusion region 19A. Diffusion region 19A is considered to be the area containing at least approximately 90% concentration of the implanted conductive atoms.

A second exemplary implementation of the present invention is depicted in Figures 2A-2G. Referring to Figure 2A, a semiconductive substrate 20, such as a silicon wafer, is prepared for the processing steps of the present invention. A first insulation layer 21 (i.e., a dielectric material such as oxide), is formed over the surface of semiconductive substrate 20. It is preferred to form the oxide by growing the oxide on the semiconductive substrate. A second insulation layer 22 (i.e., a dielectric material such as nitride) is formed over the first insulation layer 21. A masking material 23, such as photoresist, is patterned over semiconductive substrate 20 leaving an exposed portion of insulation layer 22.

Referring now to Figure 2B, an anisotropic etch is performed that etches through the exposed portion of insulation layer 22, through insulation layer 21 and continues into the semiconductive substrate 20, creating a first trench 24 therein. The desired depth of first trench 24 is discussed further in the process steps.

Referring now to Figure 2C, the masking material 23 is stripped from the substrate's surface. Next, a third insulation layer 25 (i.e., a dielectric material, such as oxide or nitride) is formed over the remaining second insulation layer 22 and next to the first trench 24 in substrate 20. (The significance of the material selected for third insulation layer 25 will become apparent from the discussion of Figures 2G and 2H.) Next, a conformal layer of dielectric material 26, such as oxide, is deposited on third insulation layer 25. As taught in the embodiment of Figures 1A-1H, the thickness of material 26 will determine the width and depth of a second trench to be subsequently formed.

Referring now to Figure 2D, the conformal layer of dielectric material 26 is anisotropically etched to remove the material from the bottom of the trench and consequently from the upper surface of the substrate. This anisotropic etch will leave behind dielectric material spacer 27 which lines the wall along the circumference of first trench 24, expose portions of insulation layer 24 at the bottom of the first trench and also expose portions on the upper surface of the substrate. During this anisotropic etch (or spacer etch in this case), as dielectric material spacer 27 is formed the spacer etch will completely clear the dielectric material from the non-trenched wafer surface, remove the now exposed portion of insulation layer 25 and also clear the material from a portion of wafer surface at the bottom of the trench. Dielectric material spacer 27 is easily formed as an anisotropic etch basically removes material in a generally vertical direction and thereby leaves behind a vertical spacer while the etch clears the semiconductive material at the bottom of the first trench.

Referring now to Figure 2E, an anisotropic etch (either the continuation of the previous anisotropic spacer etch described in Figure 2D or a separate anisotropic etch) is performed that etches into the substrate using the dielectric material spacer 27 as a self-aligning guide, to form a second trench 28. This etch will also remove more of the spacer material, however a desired trench depth is easily reached while a substantial portion of the

spacer material remains intact. The width of second trench 28 can be controlled by the depth of dielectric material layer 26.

An optional step is depicted in Figure 2F which shows the formation of a second conformal layer of semiconductive material 29 that covers the remaining portion of second insulating 22, dielectric material spacers 27 and the wall and bottom surface of second trench 28. The addition of semiconductive material 29 will provide additional oxidizable material for the following step.

Referring now to Figure 2G, isolation material 30 is formed such that it consumes semiconductive material 29 (if present) and fills both the first and second substrate trenches 24 and 30. In this embodiment, if third insulation layer 25 is substantially non-oxidizable, such as a nitride of the semiconductive material (i.e., silicon nitride is effective as it is non-receptive to oxidation) and is chemically different than the first insulation layer and the (nitride) lining of first trench 24 will prevent further oxidation of the semiconductive material about the wall of the first trench region. If the third insulation layer 25 is oxide, it will become part of isolation region 30. In order to form isolation material 30, it is preferred to anneal the entire semiconductor assembly in a furnace while in the presence of an oxidizing agent. Isolation material 30 may also be formed by the deposition of oxide to fill the trenches.

Referring now to Figure 2H, isolation material 30 may be planarized by using the remaining portion of insulating layer 22 as an etch stop. Then the remaining portion of insulating layer 22 is removed to leave a planar surface for processing the semiconductor assembly further, such as for transistor formation. The planarization of isolation material 30 will substantially reduce or possibly eliminate any encroachment of isolation material 30 at the upper corners of first trench 24. In this embodiment, planarization of isolation material 30 by etching is preferred as there is an etch stop layer (layer 25) available to use.

Figure 2I shows a relationship between the formed isolation structure 30 and bordering transistors 31. Transistors 31 comprise of transistor gates 31B bridging across diffusion regions 31A. This view demonstrates the importance of second trench 28 to obtain effective isolation between transistors 31. It is preferred that the overall depth of first

trench 24 and second trench 28 be two times the depth of diffusion region 31A. Diffusion region 31A is considered to be the area containing at least approximately 90% concentration of the implanted conductive atoms.

During a given fabrication process, implementation of any one of the embodiments of the present invention will provide a trench having the desired width and depth. In general, the disclosed methods can be used to make a second trench ½ to ¼ of the width of the upper (first) trench and is dependent upon materials utilized and the depth of deposition of those materials. For example, to create a second trench approximately 0.18 microns wide, the first trench would be etched to a width of approximately 0.3 microns. The semiconductive material would then be formed over the substrate's surface at a thickness of approximately 0.06 microns. After the spacer etch is performed, the resulting spacer formed on the sidewall of the first trench would be approximately 0.06 microns wide. Then using the spacer as an etching guide to form the second trench (as described in the above embodiments) the subsequent anisotropic etch would result in a second trench having a width of approximately 0.18 microns.

It is to be understood that although the present invention has been described with reference to several preferred embodiments, various modifications, known to those skilled in the art, such as utilizing the disclosed methods to form sub-resolution contracts, may be made to the structures and process steps presented herein without departing from the invention as recited in the several claims appended hereto.